S/N 09/945554 **PATENT**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Leonard Forbes	Examiner:	Thomas L Dickey
Serial No.:	09/945554	Group Art Unit:	2826
Filed:	August 30, 2001	Docket:	1303.028US1
Title:	SRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS		

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

In compliance with the duty imposed by 37 C.F.R. § 1.56, and in accordance with 37 C.F.R. §§ 1.97 *et. seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified patent application. Applicant respectfully requests that this Information Disclosure Statement be entered and the documents listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to the provisions of MPEP 609, Applicant requests that a copy of the 1449 form, initialed as being considered by the Examiner, be returned to the Applicant with the next official communication.

Pursuant to 37 C.F.R. §1.97(c)(2), Applicants have included the fee of $180.00 as set forth in 37 C.F.R. §1.17(p). Please charge any additional fees or credit any overpayment to Deposit Account No. 19-0743.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

LEONARD FORBES

By his Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
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(612) 349-9587

Date 22 Jan '04

By _____
Timothy B Clise
Reg. No. 40,957

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 22nd day of January, 2004.

Amy Moriarty
Name

_____
Signature

PTO/SB/08A(10-01)
Approved for use through 10/31/2002. OMB 651-0031
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Substitute for form 1449A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

Sheet 1 of 1

Complete if Known	
Application Numb r	09/945554
Filing Date	August 30, 2001
First Named Inventor	Forbes, Leonard
Group Art Unit	2826
Examiner Name	Dickey, Thomas

Attorney Docket No: 1303.028US1

US PATENT DOCUMENTS

Examiner Initial *	USP Document Number	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	Filing Date If Appropriate
	US-6,461,931	10/08/2002	Eldridge, Jerome M.	438	398	08/29/2000
	US-6,586,797	07/01/2003	Forbes, Leonard , et al.	257	325	08/30/2001

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Foreign Document No	Publication Date	Name of Patentee or Applicant of cited Document	Class	Subclass	T[2]

OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No [1]	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T[2]
		SHI, Y. , "Tunneling Leakage Current in Ultrathin (<4 nm) Nitride/Oxide Stack Dielectrics", IEEE Electron Device Letters, 19(10), (1998),pp. 388-390	
		ZHANG, "Atomic Layer Deposition of High Dielectric Constant Nanolaminates", Journal of The Electrochemical Society, 148(4),(2001),F63-F66	

EXAMINER **DATE CONSIDERED**

· EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. 1 Applicant's unique citation designation number (optional) 2 Applicant is to place a check mark here if English language Translation is attached

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COMMUNICATION CONCERNING RELATED APPLICATION(S)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicant would like to bring to the Examiner's attention the following related application(s) in the above-identified patent application:

Serial/Patent No.	Filing Date	Attorney Docket	Title
09/945507	August 30, 2001	1303.014US1	FLASH MEMORY WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/945395	August 30, 2001	1303.019US1	DRAM CELLS WITH REPRESSED FLOATING GATE MEMORY, LOW TUNNEL BARRIER INTERPOLY INSULATORS
09/943134	August 30, 2001	1303.020US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY DEVICES WITH ASYMMETRICAL TUNNEL BARRIERS
09/945498	August 30, 2001	1303.024US1	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD
09/945512	August 30, 2001	1303.027US1	IN SERVICE PROGRAMMABLE LOGIC ARRAYS WITH LOW TUNNEL BARRIER INTERPOLY INSULATORS
10/028001	December 20, 2001	1303.035US1	PROGRAMMABLE ARRAY LOGIC OR MEMORY WITH P-CHANNEL DEVICES AND ASYMMETRICAL TUNNEL BARRIERS
10/081818	February 20, 2002	1303.045US1	ATOMIC LAYER DEPOSITION OF METAL OXIDE AND/OR LOW

			ASYMMETRICAL TUNNEL BARRIER INTERPLOY INSULATORS
10/177096	June 21, 2002	1303.063US1	GRADED COMPOSITION METAL OXIDE TUNNEL BARRIER INTERPOLY INSULATORS
	Herewith	1303.024US2	INTEGRATED CIRCUIT MEMORY DEVICE AND METHOD

Respectfully submitted,

LEONARD FORBES

By Applicant's Representatives,

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Date 22 Jan '04 By _____
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Amy Moriarty
Name

Signature